REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Initially, Applicants note that with the Office Action of February 4, 2005, Applicants form PTO-1449 submitted with the previously filed Information Disclosure Statement (IDS) was returned to Applicants. However, that form apparently inadvertently omitted initialing references labeled AO-AR and AW. Applicants respectfully request a new form PTO-1449 be provided that acknowledges consideration of each of the references listed thereon.

The specification is amended by the present response to clarify the added paragraph of the Cross-Reference To Related Applications.

Claims 21-50 are pending in this application. Claim 29 was rejected under 35 U.S.C. § 112, second paragraph. Claims 21, 22, 24, 26-40, 42, and 44-50 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,923,892 to Levy. Claims 21-27 and 32-50 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,838,934 to Boutaud et al. (herein "Boutaud").

Addressing first the rejection of claim 29 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

Claim 29 is amended by the present response to now consistently refer to "the operation mode set in the first return address register". The amendment to claim 29 is believed to address the rejection thereto under 35 U.S.C. § 112, second paragraph.

Addressing now the above-noted rejections based on Levy and Boutaud, those rejections are traversed by the present response.

Initially, applicants note each of the claims is amended by the present response to clarify features recited therein. Specifically, independent claim 21 now more clearly recites that the at least one second operation processor "runs by an extended instruction supplied from the first operation processor, wherein the extended instruction includes a first code for

the first operation processor and a second code for the second operation processor". That feature is believed to be fully supported by the original specification for example in Figures 3 and 8 showing an extended instruction including first and second codes.

Independent claim 21 now also further recites, with respect to the first operation mode in which the first operation processor alone is operated, "the extended instruction comprises only the first code in the first operation mode". That subject matter is fully supported by the original specification for example in Figure 6 and the corresponding description therein in the specification.

The other independent claims 39, 49 and 50 are amended similarly as in independent claim 21 noted above.

The features recited in the claims as currently written are believed to clearly distinguish over the applied art.

With respect to the background art such as shown for example in Figures 1 and 2 in the present specification, the applicants of the present invention recognized that when a processor includes a great number of instructions that define a single operation processing, by which for example only the integer processor 1 of Figure 1 alone is to be run, the conventional processor 20 has to embed an instruction not to run any unit (no operation instruction: NOP instruction) into a portion 72 that defines an operation of the data processor 2. That is, in such a conventional art an extended instruction with two different instructions 71, 72 is utilized. However, if only one processor apparatus is to be utilized the complete extended instruction format is still utilized, and a NOP instruction must be inserted for example into a portion 72 when the data processor 2 is not to be utilized. As a result, utilization of extended instructions is reduced, and a capacity of an instruction memory for storing instructions is undesirably increased.[1]

[1] See for example the present specification at page 2, lines 6-20.

The present invention overcomes such drawbacks as in the present invention the extended instruction includes only a first code in a first operation mode, the first operation mode being a mode in which only a first operation processor alone is operated.

More specifically, in the present invention a first operation processor (host processor or integer processor) and a second operation processor (coprocessor or data processor) can be provided in a VLIW (Very Long Instruction Word) architecture. The second operation processor is operated by the extended instruction supplied from the first operation processor, as shown as a non-limiting example in Figure 3 in the present specification in which the instruction decoder 121 in the data processor 12 is provided with the instruction from the instruction memory 112 and instruction register unit 113 in the integer processor 11.

In the VLIW architecture the extended instruction includes two portions, a first code for a first operation processor and a second code for a second operation processor (see for example Figure 8 in the present specification).

As noted above, in conventional art such as in Figures 1 and 2 of the present specification the second code of the extended instruction has to be embedded with a NOP instruction for the second operation processor in a mode in which the first operation processor alone is operated. In such a situation the second code is redundant in such a first operation mode in which almost all clock cycles are spent.

In contrast, in the claimed invention the necessity for such a second code of extended instructions is eliminated. That is, in the claims as currently written a second code, such as shown for example in Figure 6, which only has a single instruction is utilized in that first operation mode. That results in allowing an instruction length to be halved in such a first operation mode.

Such features as reflected in the claims as currently written are believed to clearly distinguish over the teachings in Levy and Boutaud.

In contrast to the claimed features, in Levy the coprocessor 38 is completely independent from the host processor 22 and carries out independent instructions. In Levy the instruction cache 86 is provided within the coprocessor 38.

In contrast to such a structure in Levy, in the claimed invention the second operation processor (e.g., the coprocessor) is supplied with an extended instruction from the first operation processor (e.g., host processor). That is, in the present invention the two operation processors are not completely independent as in Levy.

Moreover, as a result of such differences between the claimed invention and the structure in Levy, in Levy there is no need to utilize a code implementation of an extended instruction including a first code for a first operation processor and a second code for a second operation processor. That is the result in Levy as the processors are independent and have independent codes provided thereto. Further, as a result of such a difference Levy does not include any operation for eliminating a second code in a first operation mode in which only a first operation processor alone is operated.

In such ways, the claims as currently written are believed to clearly distinguish over the teachings in Levy.

With respect to Boutaud, Boutaud is similar to Levy in that in Boutaud the coprocessor 300 is completely independent of the host processor 400 and carries out independent instructions. In Boutaud only a memory is shared between the processors.

In the claimed invention, in contrast to Boutaud, the second operation processor (e.g., coprocessor) is supplied with extended instructions from the first operation processor (e.g., host processor).

In Boutaud in a HOM (host only mode) in which the host 400 is allowed to access memory 200 without processor 300 being able to access memory 200, the processor 300 is set to a sleep mode or to idle independently, without needing a control signal to halt the

processor 300 from the host processor (see for example Boutaud at column 13, lines 59-65 and column 16, lines 13-28). Therefore, in Boutaud there is also no implementation of nor need for an extended instruction including a first code for a first operation processor and a second code for a second operation processor. As a result Boutaud also does not disclose any operation for being able to eliminate such a second code in a particular operation mode in which only a first operation processor is operated.

In such ways, the claims as currently written are believed to also distinguish over the teachings in Boutaud.

In view of these foregoing comments, applicants respectfully submit the claims as currently written distinguish over both Levy and Boutaud.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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